

IN THE CLAIMS:

Each of the claims that remains pending and under consideration in the above-referenced application is shown below, in clean form, for the sake of clarity. A marked-up version of each amended claim is also enclosed herewith to clearly identify each change that has been made thereto.

Please enter the claims as follows:

31. (Previously amended three times) A semiconductor capacitor storage poly, comprising:

downwardly extending recesses; and

a plurality of contiguous mesas comprising a plurality of contiguous top surfaces forming a maze-like structure.

32. The storage poly of claim 31, wherein said mesas extend in the X, Y and Z coordinates.

33. (Previously amended three times) A semiconductor capacitor storage poly, comprising:

downwardly extending recesses;

a plurality of contiguous webs comprising a plurality of contiguous top surfaces forming a maze-like structure; and

hemispherical-grain polysilicon on at least some of said plurality of contiguous top surfaces.

34. (Previously amended) The storage poly of claim 33, wherein said webs extend in the X, Y and Z coordinates.

35. (Thrice amended) An intermediate semiconductor capacitor structure, comprising:

a storage poly structure comprising a plurality of contiguous mesas with recesses therebetween;

a contiguous hemispherical-grain polysilicon layer on said storage poly structure and in contact therewith; and

a mask over said hemispherical-grain polysilicon layer, said recesses being exposed through said contiguous hemispherical-grain polysilicon layer and said mask.

37. (Twice amended) An intermediate semiconductor memory cell structure,

comprising:

a storage poly structure;

a plurality of contiguous low elevation regions of a hemispherical-grain polysilicon layer on said storage poly structure;

recesses formed in said storage poly structure and located laterally between said plurality of contiguous low elevation regions of said hemispherical-grain polysilicon layer; and dielectric material at least lining the recesses.

38. (Previously amended) A semiconductor memory cell structure, comprising:

a storage poly structure;

regions of hemispherical-grain polysilicon on at least portions of an upper surface of said storage poly structure;

a plurality of recesses extending into said storage poly structure, at least some recesses of said plurality of recesses being located laterally between said regions of hemispherical-grain polysilicon; and

and a dielectric layer substantially coating an upper surface of said storage poly structure and substantially lining each of said plurality of recesses.

39. The semiconductor memory cell structure of claim 38, further comprising a cell poly structure over said dielectric layer.

40. (Previously amended twice) The semiconductor memory cell structure of claim 38, wherein said storage poly structure comprises a web-like structure comprising a plurality of contiguous top surfaces.

41. The semiconductor memory cell structure of claim 38, wherein at least some of said plurality of recesses extend into said storage poly structure.

42. (Previously amended) An intermediate semiconductor capacitor structure, comprising:

a storage poly structure;
a substantially confluent hemispherical-grain polysilicon layer on said storage poly structure; and
a mask positioned over said substantially confluent hemispherical-grain polysilicon layer,
elevated portions of said hemispherical-grain polysilicon layer being exposed through said mask.

43. (Thrice amended) An intermediate semiconductor capacitor structure, comprising:
H³
a storage poly structure including recesses therein;
remaining portions of a hemispherical-grain polysilicon layer substantially overlying upper portions of said storage poly structure; and
a mask positioned over said hemispherical-grain polysilicon layer, laterally between said recesses, and substantially spaced apart from said storage poly structure by said remaining portions of said hemispherical-grain polysilicon layer, said recesses in said storage poly structure being exposed through said mask.

44. (Amended four times) An intermediate semiconductor capacitor structure, comprising:
H⁴
a storage poly structure with recesses therein;

a hemispherical-grain polysilicon layer on at least portions of the storage poly structure; and dielectric material lining at least said recesses.

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45. (Amended twice) An intermediate semiconductor memory cell structure, comprising:
a storage poly structure with recesses therein;
low elevation regions of a hemispherical-grain polysilicon layer on at least portions of the storage poly structure; and
dielectric material at least lining said recesses.